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FIG. 1

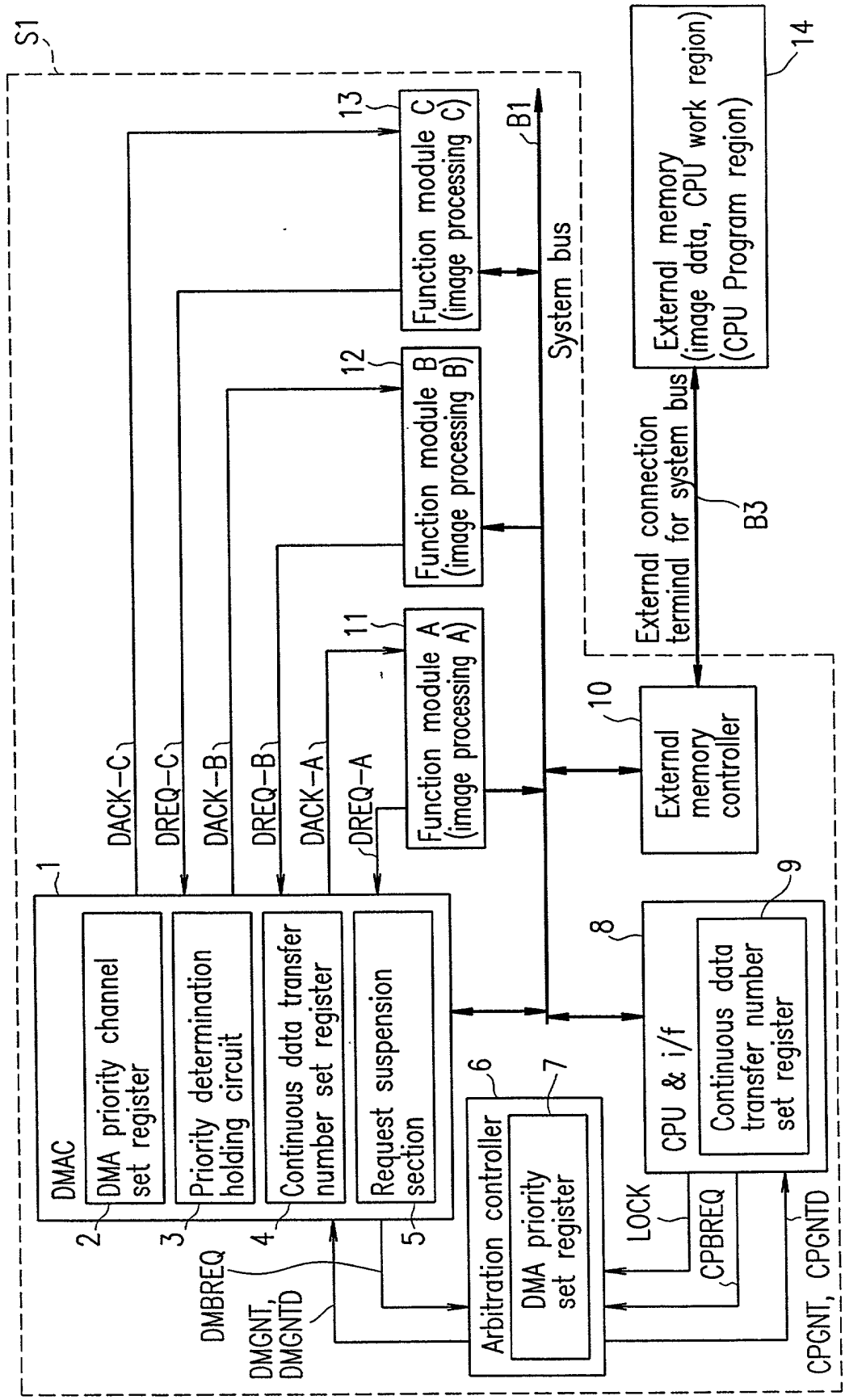

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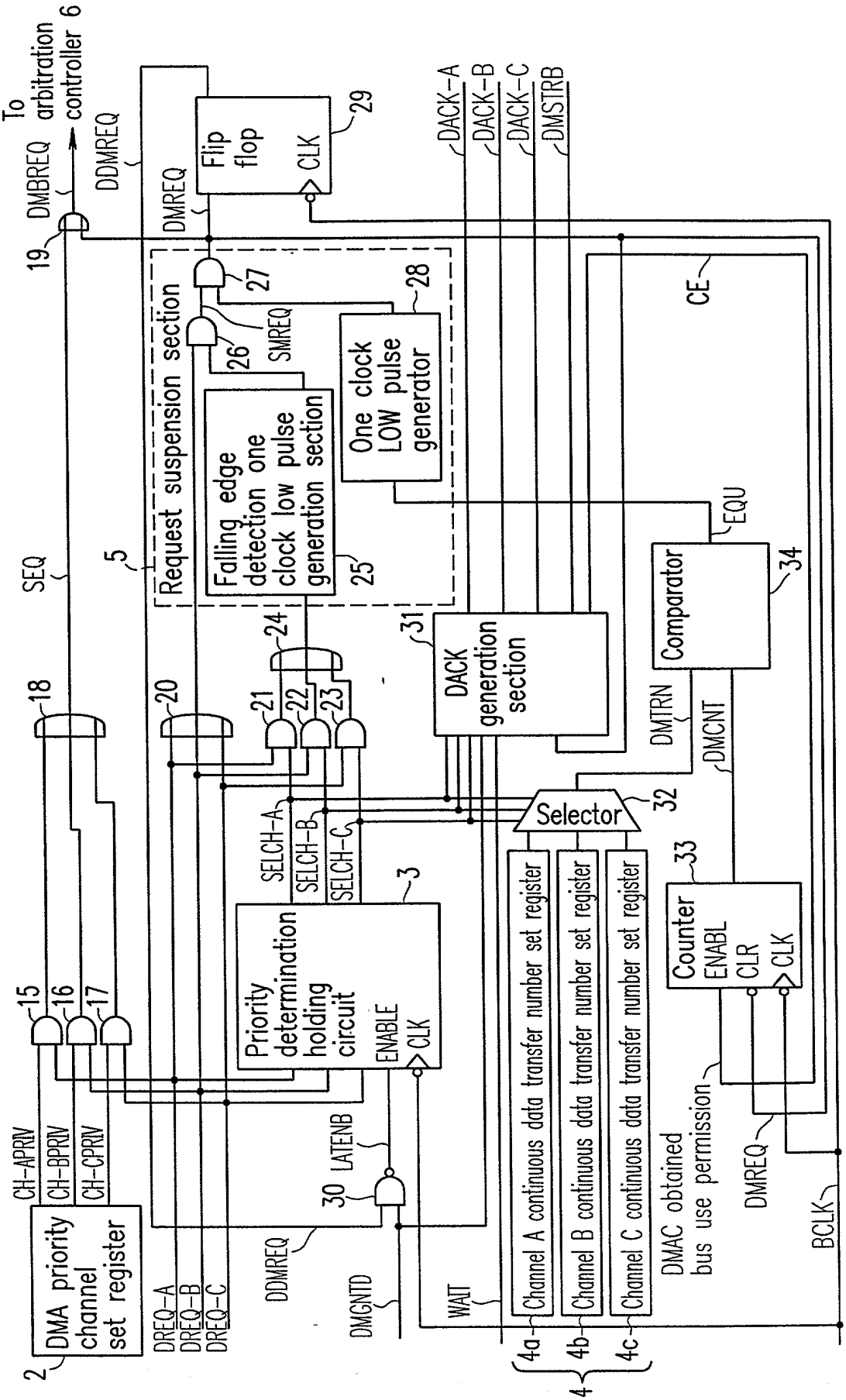
FIG. 2



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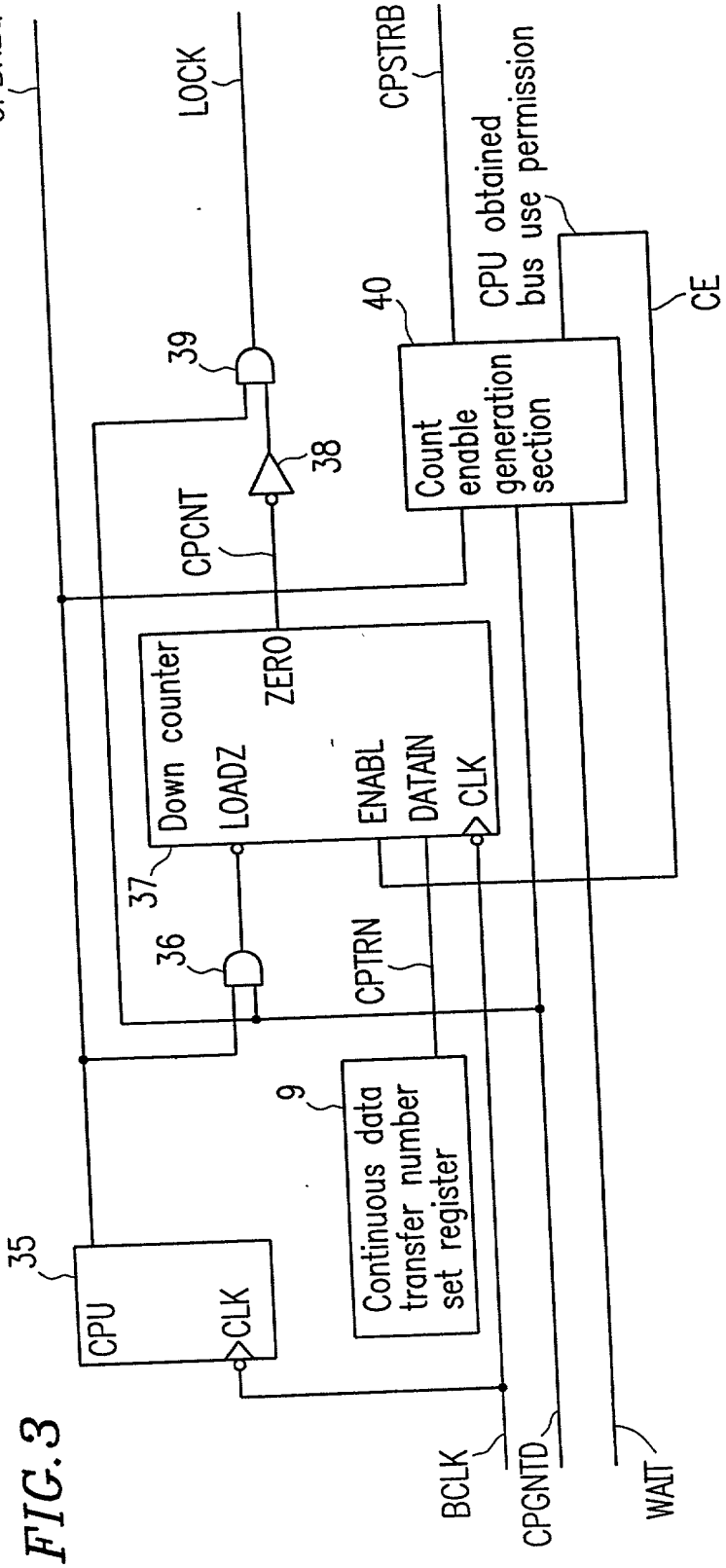


FIG. 3

FIG. 4

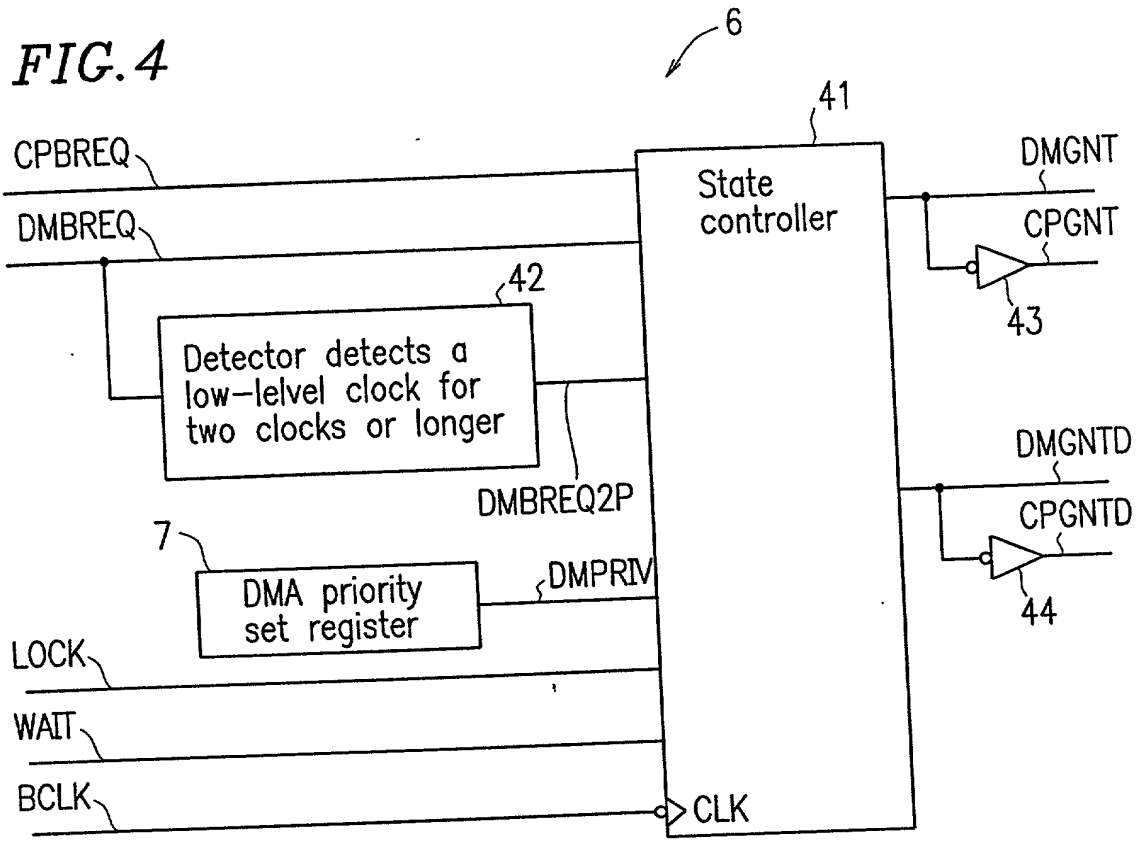
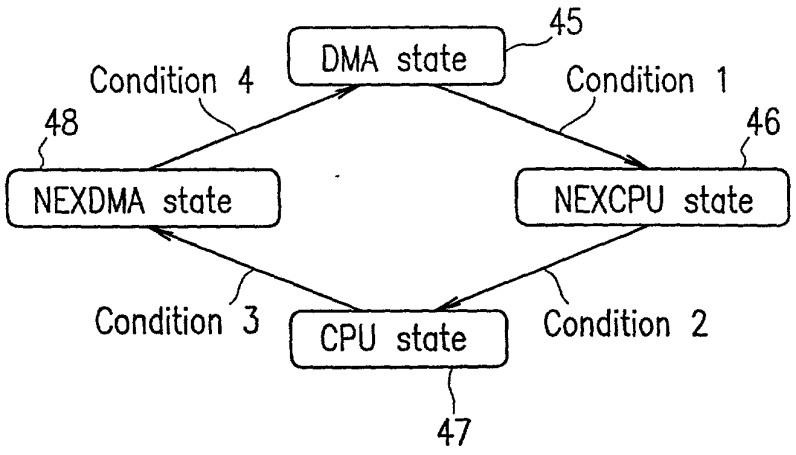

6
41
CPBREQ
DMBREQ
State controller
DMGNT
CPGNT
43
42
Detector detects a low-lelvel clock for two clocks or longer
DMBREQ2P
DMGNTD
CPGNTD
44
7
DMA priority set register
DMPRIV
LOCK
WAIT
BCLK
CLK

FIG.5



State transition condition
(Transition occurs when each condition is satisfied)

Condition 1: CPBREQ & ((!DMPRIV & !DMBREQ) or (DMPRIV & DMBREQ2P))
Condition 2: !WAIT (not in WAIT state)
Condition 3: DMBREQ
Condition 4: !(LOCK & CPBREQ) & !WAIT (not LOCKed and not in WAIT state)

State Definition
(output levels of signals for each state)

DMA : DMGNT = High, DMGNTD = High
NEXCPU: DMGNT = Low, DMGNTD = High (Bus use permission is transferred to CPU in next cycle)
CPU : DMGNT = Low, DMGNTD = Low
NEXDMA: DMGNT = High, DMGNTD = Low (Bus use permission is transferred to DMAC in next cycle)

[NOTE] Meanings of above symbols are as follows:

& ··· logical multiplication
or ··· logical sum
! ··· inversion of logic

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FIG. 6

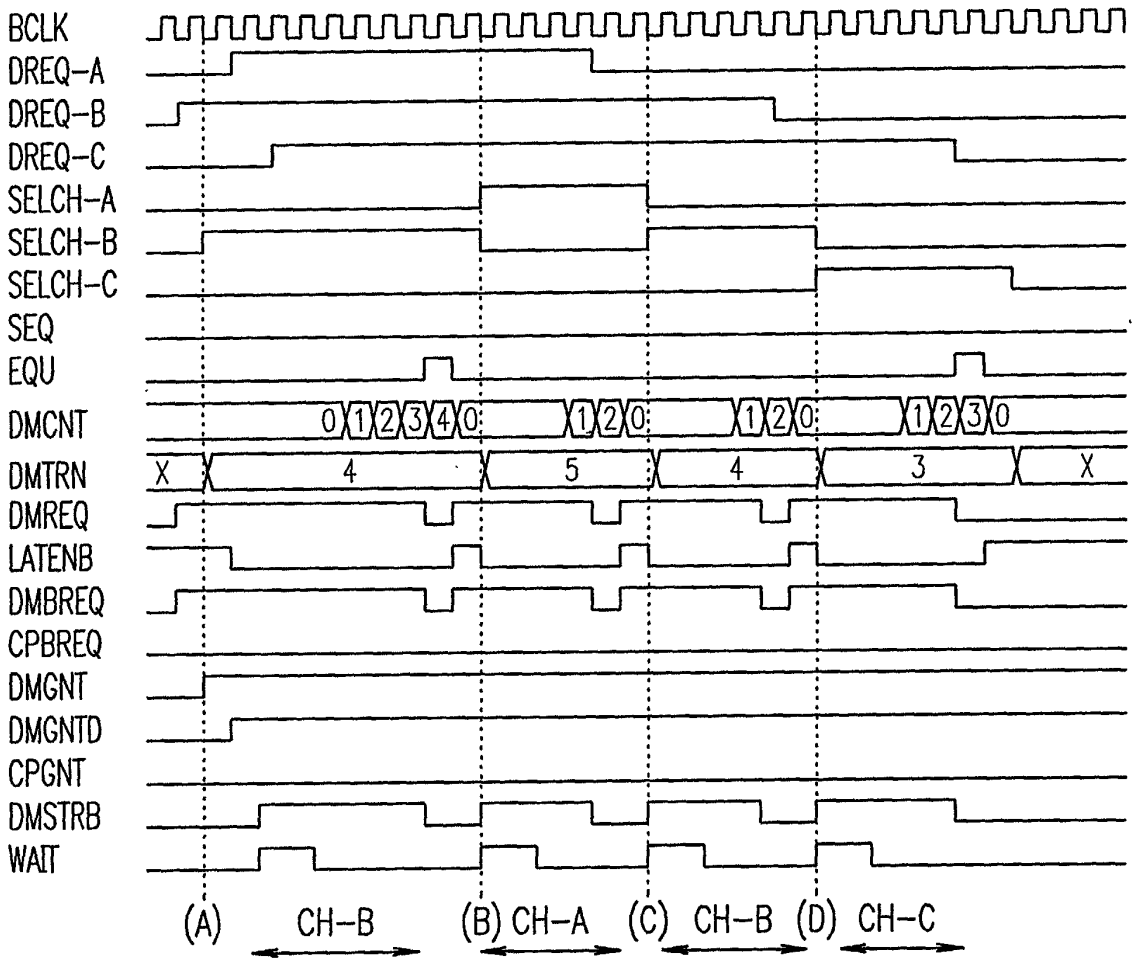

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FIG. 7

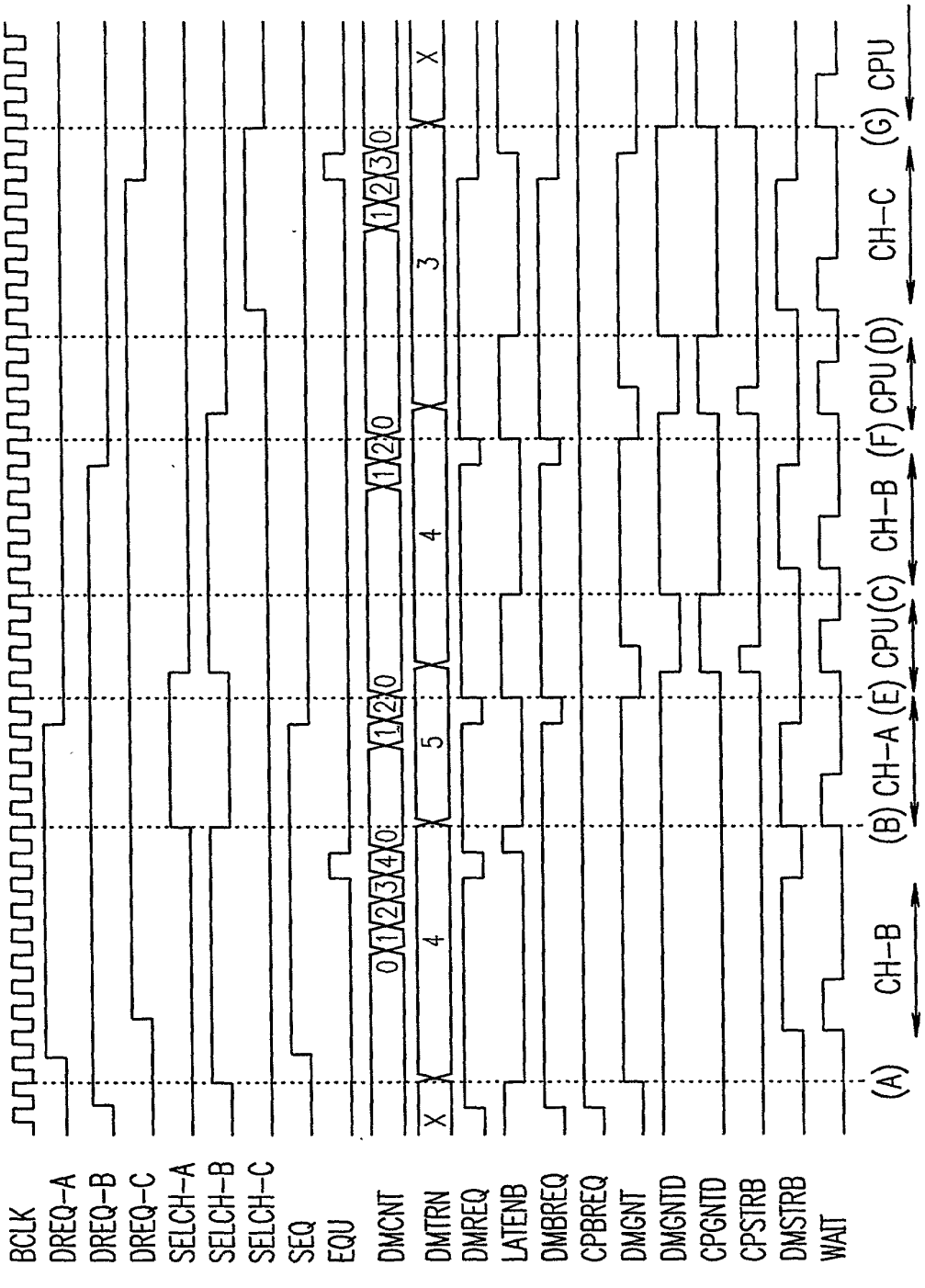
BCLK
DREQ-A
DREQ-B
DREQ-C
SELCH-A
SELCH-B
SELCH-C
SEQ
EQU
DMCNT
DMTRN
DMREQ
LATENB
DMBREQ
CPBREQ
DMGNT
DMGNTD
CPGNTD
CPSTRB
DMSTRB
WAIT
(A) CH-B
(B) CH-A
(E) CPU
(C) CH-B
(F) CPU
(D) CH-C
(G) CPU

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FIG. 8

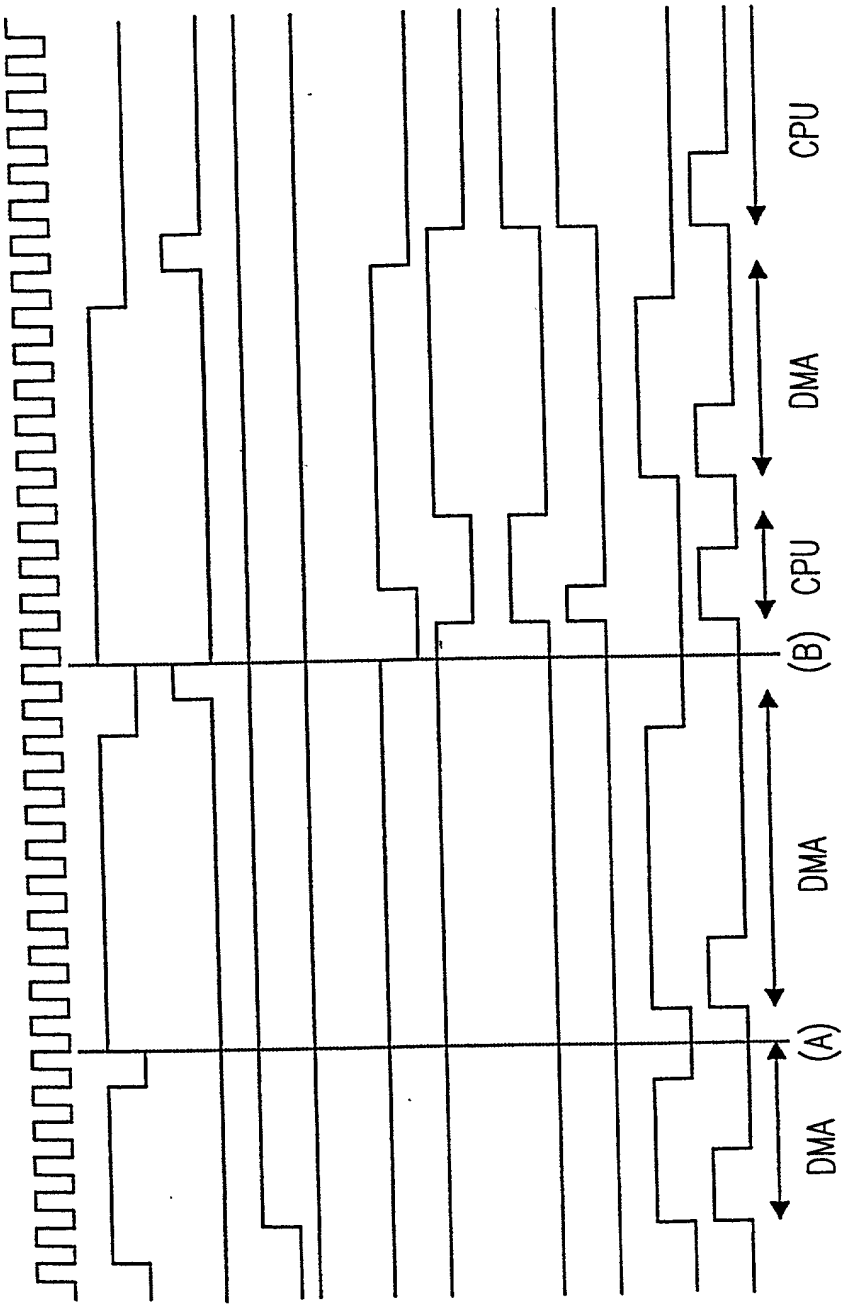

FIG. 9

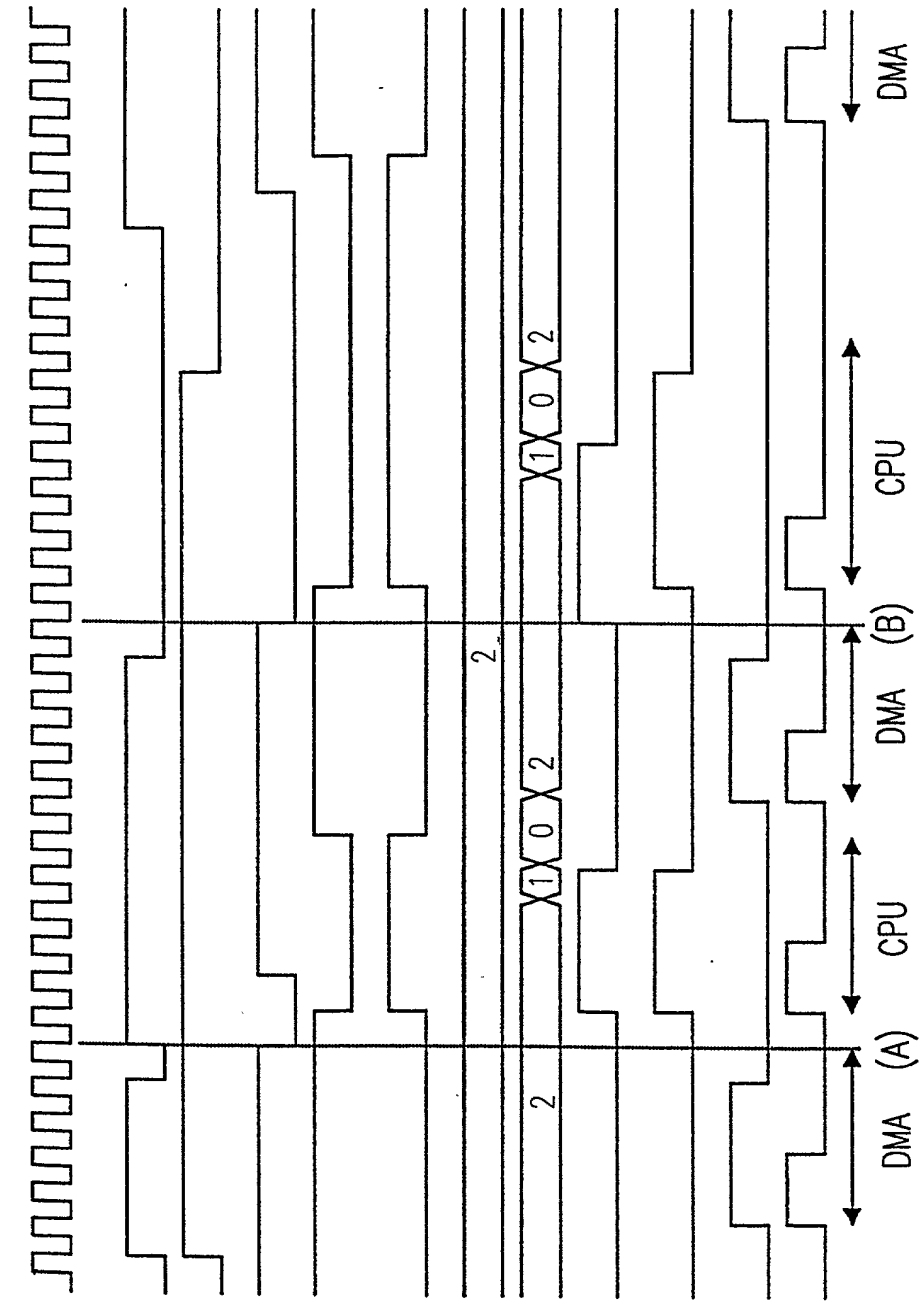
BCLK
DMBREQ
CPBREQ
DMGNT
DMGNTD
CPGNTD
CPTRN
CPCNT
LOCK
CPSTRB
DMSTRB
WAIT
2
X1X0X2
DMA (A)
CPU
DMA (B)
CPU
DMA

FIG. 10

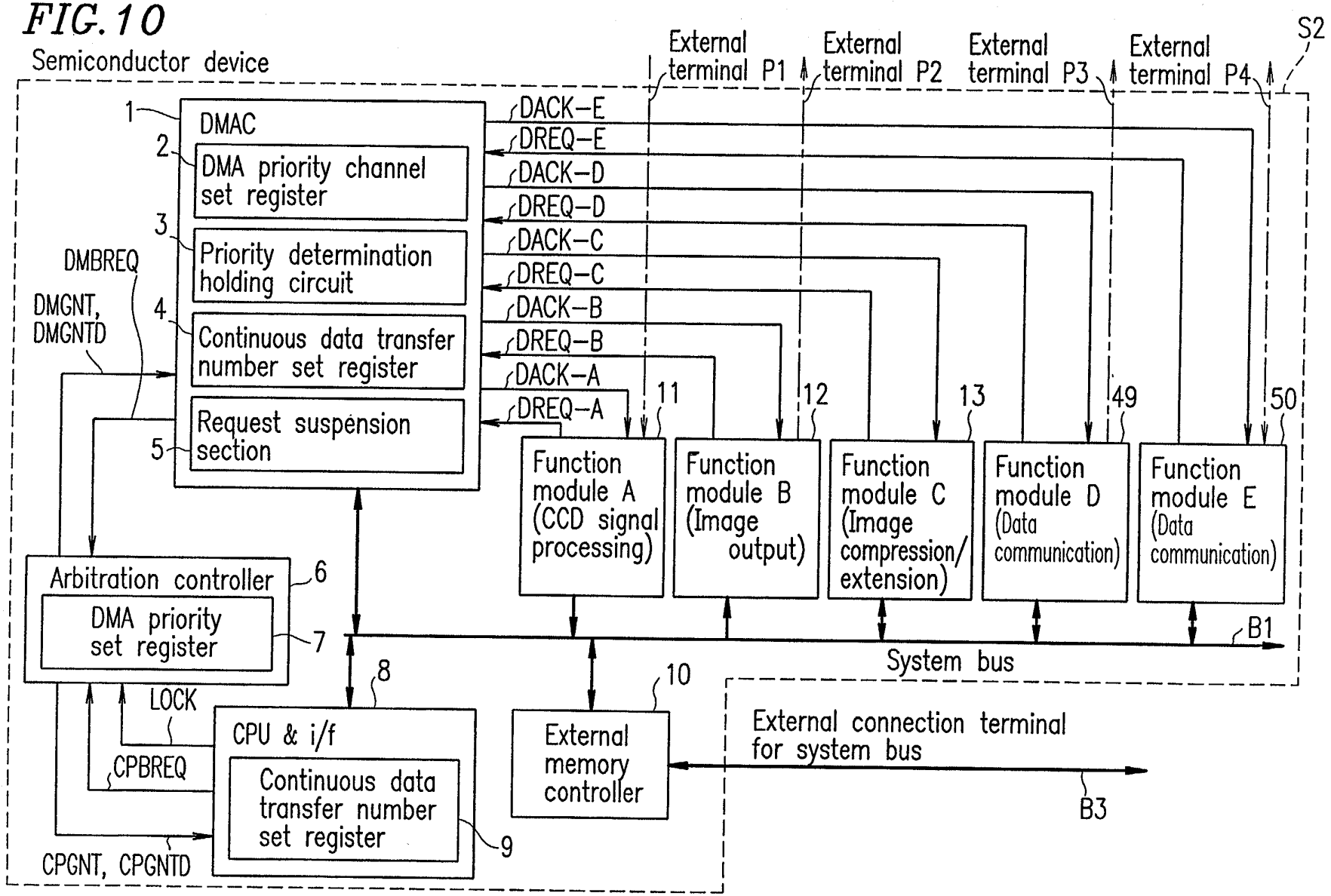

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FIG. 11

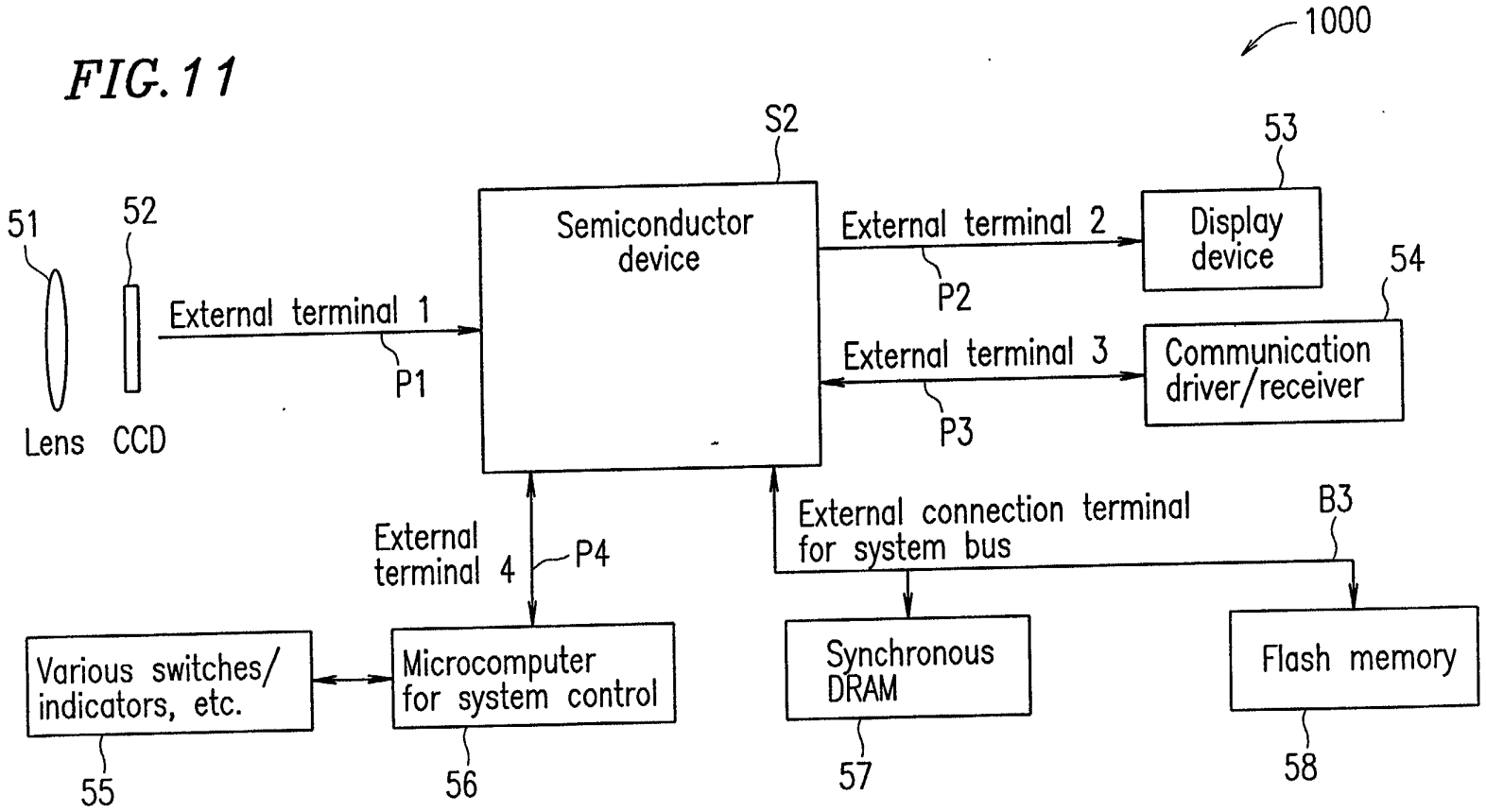

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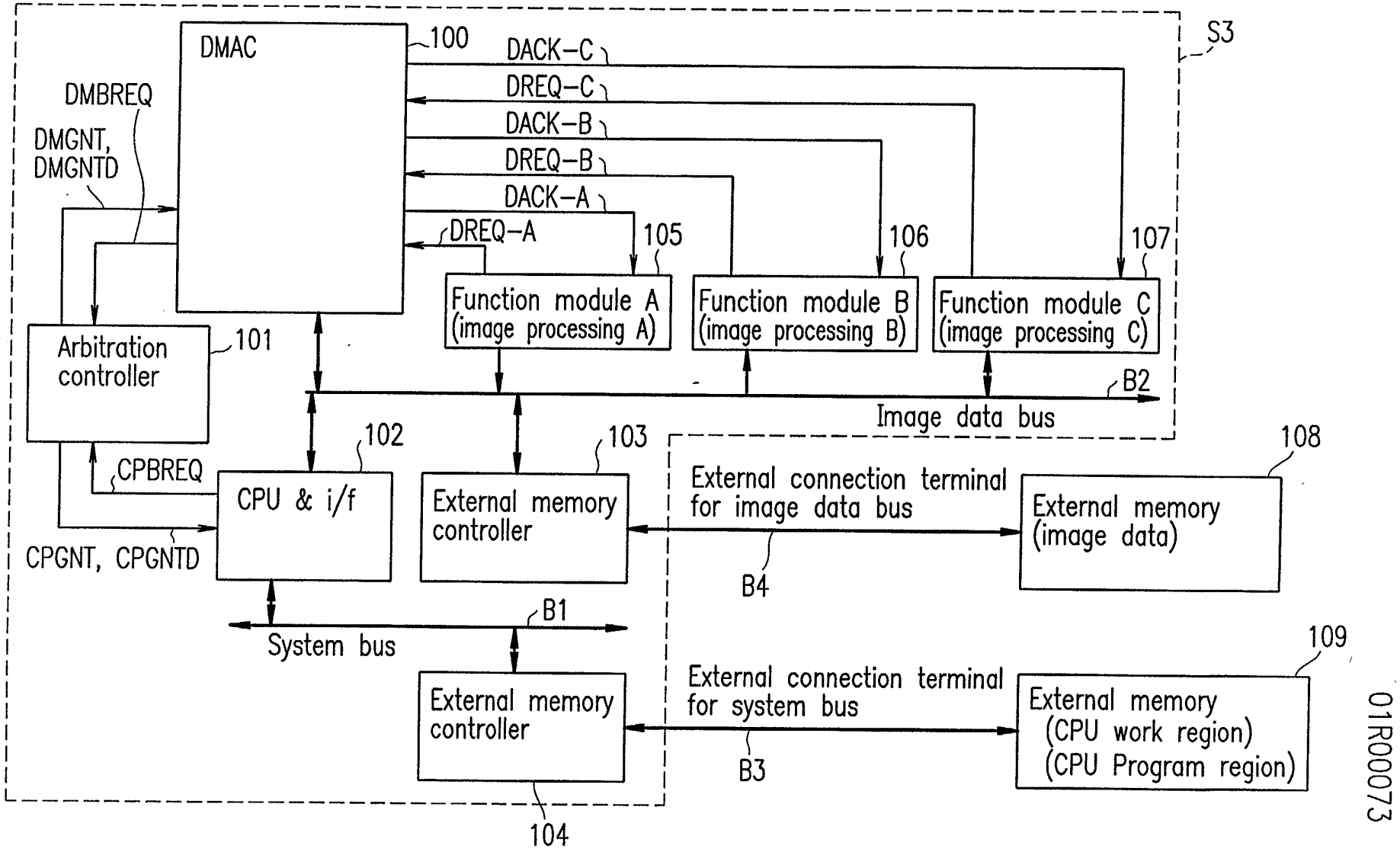
FIG. 12



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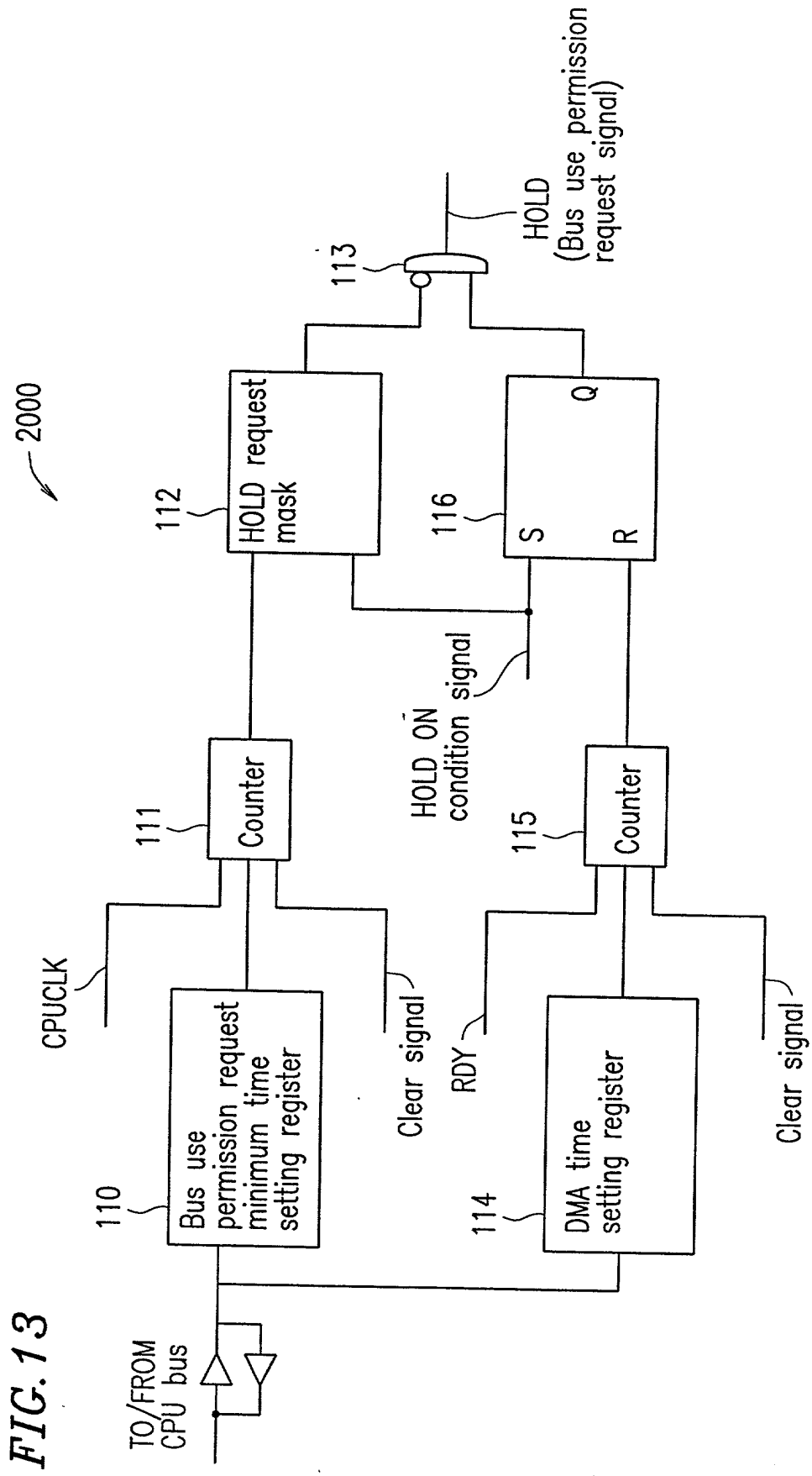

FIG. 13

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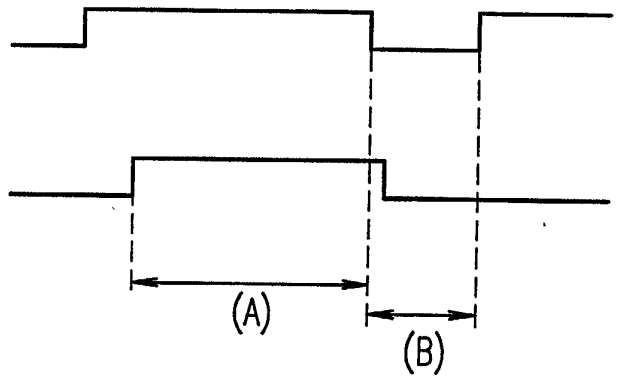
FIG. 14

(1) HOLD
(bus use permission request signal)

(2) HOLDACK
(bus use permission signal)



(A) DMA transfer time
(CPU or DMAC which has bus use permission uses bus for data transfer)

(B) Bus use permission request minimum time
(time consumed until a bus use permission can be requested after the data transfer during time (A) is completed)

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